האוניברסיטה העברית בירושלים
THE HEBREW UNIVERSITY OF JERUSALEM

הפקולטה למתמטיקה ולמדעי הטבע
Faculty of Science

HUJI Dept. of Applied Physics

A Special Dept. Seminar

Monday, February 10 2020, At 11:00

Bergman Bldg., Seminar Hall

Refreshments will be served at 10:45

"Application Oriented Alternative Embedded Memories"

Speaker: Dr. Robert Giterman

École Polytechnique Fédérale de Lausanne

Abstract: **Modern industry growth drivers, such as Artifcial Intelligence (AI) and machine learning, 5G, Internet-of-Things (IOT), and automotive, require ever increasing amounts of on-chip memories in order to minimize bandwidth limiting and power-dominant off-chip memory accesses. In fact, today, the amount of embedded memory on almost any system-on-a-chip (SoC) is reaching hundreds of megabits, accounting often for up-to 80% of the total chip area. Static random access memory (SRAM) has been the traditional choice for embedded memory since it provides high-speed read and write operations and static data retention. However, the 6-Transistor (6T) SRAM bitcell is relatively large, exhibits several leakage paths, and has dramatically increased failure rates under voltage scaling. Gain-Cell embedded DRAM (GC-eDRAM) has recently emerged as an alternative to conventional embedded memories based on SRAM, as it offers high density, low leakage power consumption, two-ported operation, and full logic-compatibility. The main drawback of GC-eDRAM compared to SRAM is the need for periodic refresh operation due to the dynamic nature of data storage.**

This talk will review recent advancements in the field of embedded memories in both circuit and architecture levels, focusing on GC-eDRAM as an emerging alternative to SRAM. Implementations of novel memory architectures in both mature (65nm) and advanced process nodes (28nm – 16nm) will be presented, targeting a wide range of applications, from low-power IoT systems, to high-density ASICs for high performance, error-resilient systems.

About the speaker: **Robert Giterman received the Bachelor's and Master's degrees in Electrical and Computer Engineering from Ben-Gurion University, Be'er Sheva, Israel, in 2013 and 2014, respectively, as part of a fast track program for outstanding students. He completed his Ph.D. degree in 2018 under Prof. Alex Fish and Dr. Adam Teman as part of the Emerging Nanoscaled Intergrated Circuits and Systems (EnICS) Laboratory in Bar Ilan University, Ramat-Gan, Israel. Since November 2018 he is a post-doctoral researcher in the Telecommunications Circuits Laboratory in EPFL.**

Mr. Giterman's research interests include embedded memory design and optimization for low power and high performance operation, error-correction and fault-tolerant circuits, development of hardware-security oriented embedded memories for use in low-power applications and high-end processors, and memory accelerators for machine learning. As part of his research, he led several full test chip integrations and tape outs. He has authored/co-authored over 30 journal articles and international conference papers and 7 patent applications, and has presented his research at a number of international conferences. He is also the co-author of the book ``Gain-Cell Embedded DRAMs for Low-Power VLSI Systems-on-Chip''.

If you are interested in meeting with the speaker, please contact Galia Shneor–galiashn@savion.huji.ac.il